Published by IOP Publishing for Sissa Medialab

Received: *October 24, 2021*
Revised: *January 14, 2022*
Accepted: *February 3, 2022*
Published: *April 20, 2022*

Topical Workshop on Electronics for Particle Physics 2021
20–24 September, 2021
Online

Versatile free-running ADC-based data acquisition system for particle detectors

L. Jokhovets,[a,*] P. Kulessa,[a,b] A. Erven,[a] C. Grewing,[a] T. Hahnraths von der Gracht,[a] M. Harff,[a] H. Ohm,[a] K. Pysz,[c] J. Ritman,[a,b,d] C. Roth,[a] M. Schlösser,[a] T. Sefzick,[a] V. Serdyuk,[a] S.v. Waasen[a] and P. Wintz[a]

[a] *Forschungszentrum Jülich, D-52428 Jülich, Germany*
[b] *GSI, D-64291 Darmstadt, Germany*
[c] *Institute of Nuclear Physics PAN, 31-342 Krakow, Poland*
[d] *Ruhr-Universität Bochum, D-44801 Bochum, Germany*

E-mail: l.jokhovets@fz-juelich.de

Abstract: A high-density and low-power (<300 mW/channel) data acquisition (DAQ) system integrating 2240 readout channels inside a single OpenVPX crate is presented. It is intended to be used in various applications, e.g. gaseous or scintillator-based particle detectors. 14 payload slots, controller and data concentrator communicate via a multi-gigabit backplane. Each payload slot consists of a front module for digital and a rear transition module for analog processing. A pair of modules implements 160 full readout chains including amplification/shaping, sampling, and feature extraction. The sampling rate and ADC resolution are configurable for 100–1000 MS/s and 14–8 bit, respectively. To extract the pulse arrival time we used a proper shaping of signals and a timing algorithm based on a non-linear rise approximation, which strongly reduces the sampling phase error, thus providing a good performance at moderate (100–250 MS/s) sampling rates. This allows raw data acquisition, arrival time extraction, energy calculation, and pile-up reconstruction for all 160 channels to be implemented in a single FPGA. It occupies less than 30% of its processing resources. The system was tested using the proton beam at COSY (Cooler Synchrotron) at Juelich Research Center (Germany). An off-detector DAQ with a 12-m long cabling was investigated. It introduces considerable additional thermal noise and crosstalk affecting the timing performance. For a sampling rate of 150 MS/s, the time resolution was found to be about 270 ps.

Keywords: Data acquisition circuits; Data processing methods; Front-end electronics for detector readout; Analogue electronic circuits

*Corresponding author.

https://doi.org/10.1088/1748-0221/17/04/C04022

Contents

1 Introduction

Modern large gaseous detectors, such as drift chambers for particle physics experiments or positron emission tomography (PET) scanners, where scintillating crystal detectors of γ-photons are used, include several tens of thousands of electronic channels [1, 2]. One of the basic requirements for those detection systems is a good time resolution. For the gaseous detectors, an uncertainty of ~1 ns in the pulse arrival times is sufficient [1, 3]. For medical PET applications, like a whole-body scanner, achieving a sub-100 ps coincidence time resolution would be very beneficial [4]. Another important system requirement is the real-time feature extraction, including the pile-up reconstruction needed at high count rates. In addition, an off-detector electronics would be advantageous, because it does not induce electromagnetic noise and heating in the sensor region. Further issues like integration level, flexibility in handling various effects, ease of implementing new processing techniques, etc. may also play a noticeable role in the design of multichannel modules.

Currently, 16–64 channel 125 MS/s digitizers are commercially available that can perform a real-time pulse processing using a field-programmable gate array (FPGA) [5]. Generally, a GS/s range of sampling rates is considered to be necessary to achieve a higher timing performance [6]. However, these sampling rates will ultimately lead to a reduced channel density. The aim of this work is to increase the number of channels assembled on the standard 6U Eurocard while simultaneously maintaining a high time resolution. A central prerequisite of our strategy is the processing algorithm introduced in [7], which uses a non-linear rise approximation. It strongly reduces the sampling phase error (SPE), and provided that the signal-to-noise ratio is sufficiently large, yields a time resolution better than $1/100^{\text{th}}$ of the sampling period. Thus, moderate sampling rates (100–250 MS/s) can be used which optimally matches the FPGA capabilities allowing us to develop a compact data acquisition (DAQ) with a high channel density and low power consumption per channel. In section 2 we present our DAQ system with off-detector electronics, including the

2022 JINST 17 C04022

description of its architecture, main blocks and functions as well as an FPGA implementation of data acquisition and their analysis. Tests of the system and its significant characteristics are discussed in section 3.

2 System with off-detector electronics

2.1 Architecture

Our system (see figure 1) is currently engaged to support experiments at COSY (Cooler Synchrotron) at Juelich Research Center (Germany). A straw-tube gaseous detector is used. Signals from the straw tubes are transferred via 12-m long thin micro coax cables (MK 5001) to a separate high voltage (HV) coupling crate. The full band of these cables is isolated additionally with an unbroken grounded aluminium foil. The DAQ crate contains a backplane (Elma VITA65), 14 payload slots, and 2 switch slots. Analog and digital modules are plugged from both sides of the crate: an analog module as a rear transition module (RTM) and a digital payload module (PLM) as a front board. Detector signals are transferred from the HV crate to each RTM via 5 flat 32-pin micro coax Samtec cables. The RTM includes 160 amplification and shaping channels. The backplane connects each RTM via 160 differential lines to a corresponding PLM where the sampling and digital processing take place. Thus, one pair of modules provides 160 full chains, and a single 19″-crate offers 2240 channels.

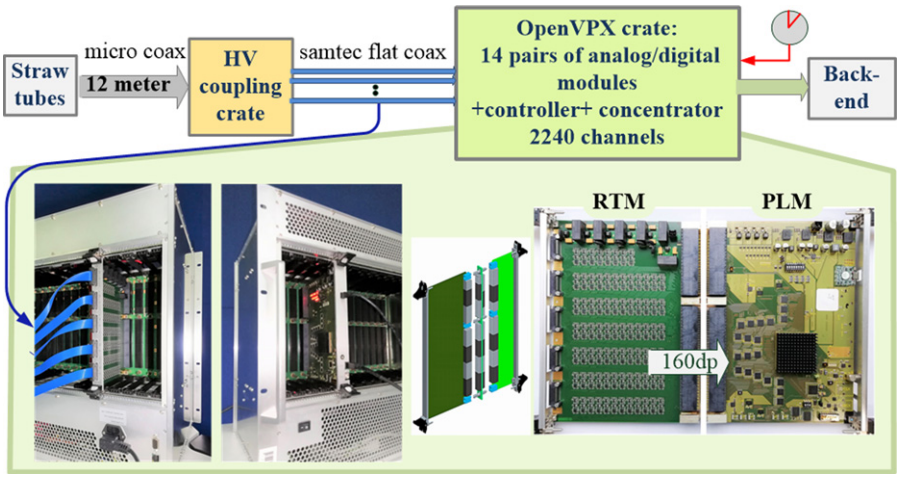


Figure 1. System structure with off-detector electronics.

2.2 Analog and digital boards

Each analog chain includes a low-noise transimpedance amplifier (Texas Instruments OPA847) and a CR-RC^2 pulse shaper. A total gain of 20 mV/μA (400 V/V) was chosen, in accordance with data for the collected charge due to ionizing particles [3]. The shaping circuit provides a 10-ns pulse peaking time. The contribution of the 12-m signal cable is of ~10 ns. Thus, the analog

2022 JINST 17 C04022

electronics results in a peaking time of approximately 20 ns. This estimation is in good agreement with a peaking time of about 23 ns observed in our test measurements using ^{55}Fe x-ray irradiation which generates nearly point-like ionization clusters. Employing a separate RTM for the analog electronics makes it easy to change the gain and shaping parameters and to modify the module, if necessary, according to the requirements of a specific application.

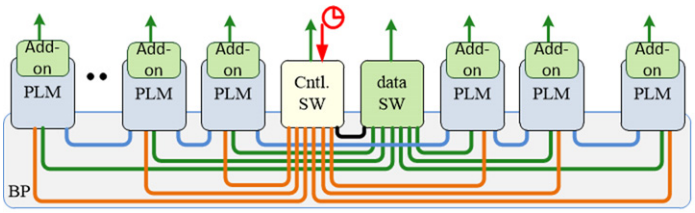
On the digital board, there are 40 four-channel analog-to-digital converters (ADCs) (Analog Devices HMCAD1520) surrounding a Virtex-7 FPGA (Xilinx XC7V585T). Signal traces from the Samtec connectors at the RTMs to the ADCs at the PLMs are length-matched. This facilitates a test of the system and permits to use it as an oscilloscope. The ADCs offer sampling rates in a range from 100 MS/s to 1 GS/s. In our design, moderate (100–250 MS/s) sampling rates are used, which are optimally matched to the FPGA operation clock. In addition, the ADCs transfer data through only two serial 1-Gb/s links, and the FPGA is capable to capture data up to same rate at its input/output (I/O) pins. This maximizes the channel density. In our DAQ system all 160 data streams are processed by a single FPGA.

The digitized signals arrive at the FPGA with a low (<80 ps) channel-to-channel skew caused by the sampling clock skew (<40 ps) and a 10-mm routing tolerance of the ADC-to-FPGA traces. Therefore, the data streams are captured without setting individual I/O delays, with equal clock phases set by a mixed-mode clock manager, and in the double data rate mode. For a sampling rate of 150 MS/s, a 12-bit ADC resolution and two output lines per channel, the serial bit rate amounts to 0.9 Gb/s. A proper clock phase is in a range from −45 to −135 degrees which corresponds to an open eye of ~700 ps.

The total power per channel consumed by the FPGA, ADCs and amplifier amounts to 50 mW + 125 mW + 100 mW = ~300 mW.

2.3 Uplinks

The backplane connects each PLM to switch slots and to the adjacent PLMs via differential pairs (figure 2). The transfer rate is determined by the connection to the FPGA: either to the 10-Gb/s multi-gigabit transceivers or to the 1-Gb/s I/O pins. In the star configuration, data are moved from the PLMs via the backplane through the switch cards. In the chain configuration the system is capable to run without the switches, and one of the PLMs takes over a master function. Each PLM can also transfer data via the USB 3.0 link (currently used) or via four 10-Gb/s small form factor pluggable connectors, which are foreseen on an add-on board of the PLMs. The sampling clock can be selected from the control switch or from one of the adjacent PLMs (via the backplane), from an on-board oscillator, and from an external source via the add-on board.



	Differential pairs at backplane				
	Total	Data 10 Gb	Data 1 Gb	GPIO 1 Gb	Clock, ctrl., 1 Gb
	16	4	8	4	
	8		8		
	8	4			4
	16	12			4

Figure 2. OpenVPX backplane. On the right: number of differential pairs in each group and their use.

2022 JINST 17 C04022

The FPGAs at the PLMs perform a real-time processing, and the PLMs communicate with each other in real time also (blue lines in figure 2). It allows all the 14 PLMs to be considered as a single real-time running unit. Thus, time sorting, clustering, pre-tracking and coincidence search operations are simplified. The system can run with an external trigger as well as in an event-triggered mode. Moreover, it can serve as a trigger for other particle detectors.

2.4 FPGA implementation of data acquisition and analysis

The acquisition of raw data, arrival time extraction, energy calculation, and pile-up reconstruction for all 160 channels are implemented in a single FPGA occupying less than 30% of its processing resource. The algorithm employed to extract the pulse arrival time has been discussed in detail previously [7]. It uses two very first samples on the pulse leading edge and the non-linear rise approximation. To implement it, a Xilinx LogiCORE IP Divider Generator core for integer division based on the LUTMult algorithm [8] is applied.

The implemented procedure of the pile-up reconstruction is valid for pile-ups where the second pulse arrives after the leading pulse has reached its maximum. Furthermore, both pulses are assumed to possess comparable amplitudes. In this case, two peaks and a well-pronounced minimum between them are observed. To determine the leading edge of the second pulse, three measured samples are used: the closest one to the minimum and the two preceding ones. Further details and experimental verification of this approach will be presented elsewhere.

3 Tests

Experimental data discussed below were obtained at a sampling rate of 150 MS/s. An off-line graphical interface (GUI) is used to observe simultaneously all 160 channels of a pair of RTM/PLM modules. At first, FPGA data capture is tested by setting all ADCs to deliver a ramp pattern. It appears as a single stepping line in the GUI. Then the ADC noise is tested. If the RTM is not inserted, the noise is approximately one least-significant bit peak-to-peak. With the RTM inserted, the noise (ADC + amplifier) increased to 4–5 bins (~0.7 mV rms). It is also possible to perform a fast test of all 160 full chains at once. If the five Samtec cables are connected to the RTM and other cable ends are open, the cables act as antennas. Random external electromagnetic interference causes weak signals to be detected. As shown in figure 3(a), there are five different signal groups corresponding to the five cables. The signals within each group are close to each other, showing that there is a proper synchronization and all 160 chains are working correctly. If the straw tubes are connected via the 12-m cable, the peak-to-peak noise increases to about 13 bins, i.e., ~1.7 mV rms. Estimation of the thermal noise caused by the cable (serial resistance of 10 Ohm) together with the impedance-matching serial 50-Ohm resistor at the input of the transimpedance amplifier gives a value of ~1.2 mV rms, which is comparable to the observed noise.

2022 JINST 17 C04022

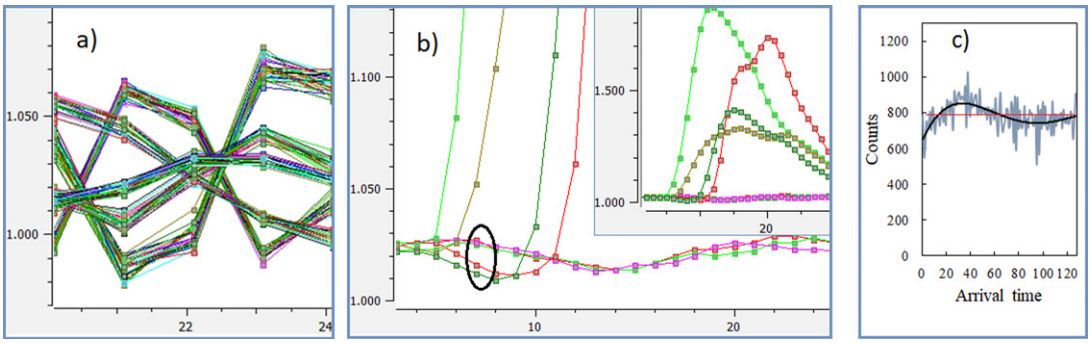


Figure 3. (a) Signals from 5 signal cables with open ends. (b) Distortions due to the crosstalk effect. The inset shows a whole signal range. (c) Arrival time histogram. The thick solid line is a fit to the data. Time on the horizontal axis is given in units of the sampling period (a) and (b) and in units of 1/128 of the sampling period (c).

To illustrate the influence of the long cabling, a section of data measured using the proton beam is shown in figure 3(b). Fluctuations of the baseline are observed due to crosstalk from the adjacent channels. Their amplitude is a factor of ~30 lower than the amplitude of the particle signals. The crosstalk can also affect the rising edges of the particle signals, thereby diminishing the reliability of the arrival time determination. Its impact can be minimized if a baseline restoration is performed, taking the signals in the adjacent channels into account.

Figure 3(c) shows a histogram of arrival times for a large (about 100,000) number of pulses, with the bin width being equal to 1/128 of the sampling period T. Note that the actual arrival times are modified by subtracting multiples of T, so all of them fall into a time interval from zero to T. The thick solid line is a 4th-order polynomial fit to the data. The observed long-wavelength fluctuation around the mean value (thin solid line) is related to the SPE. Based on these data, the latter is estimated to be of ~200 ps. Short-wavelength fluctuations around the thick solid line are caused mainly by the digitization of raw data and the divider discretization. The timing error due to the electronic noise introduced by the 12-m long signal cable is ~180 ps, as estimated using simulation results of ref. [7]. Thus, the total timing error amounts to ~270 ps.

4 Conclusion

We have developed a high-density (160 channels assembled on the standard 6U Eurocard) and low-power (~300 mW/channel) DAQ system for particle detectors with off-detector electronics. The raw data acquisition, extraction of the pulse arrival time, energy calculation, and pile-up reconstruction are implemented in a single FPGA and run in real time for all 160 channels independently. For the data analysis we have used a highly-effective algorithm based on a non-linear rise approximation that provides a good time resolution at moderate (100–250 MS/s) sampling rates. Tests of the system showed that the cabling leads to a noticeable degradation of the timing performance, mainly due to the additional thermal noise and crosstalk effects. For a 12-m long cable, the time resolution has an acceptable value of ~270 ps.

2022 JINST 17 C04022

Considering the ease of implementing new pulse-processing techniques and flexibility in handling various effects, it can be concluded that the approach presented here may have a wide applicability.

References

[1] G. Visser et al., *A 72 channel 125 MSPS analog-to-digital converter module for drift chamber readout for the GlueX detector,* in *IEEE Nuclear Science Symposuim & Medical Imaging Conference* (2010), pp. 777–81.

[2] S. Vandenberghe, P. Moskal and J.S. Karp, *State of the art in total body PET, EJNMMI Phys.* **7** (2020) 35.

[3] D. Przyborowski et al., *Development of a dedicated front-end electronics for straw tube trackers in the PANDA experiment,* 2016 *JINST* **11** P08009.

[4] P. Lecoq, *Pushing the limits in time-of-flight PET imaging, IEEE Trans. Radiat. Plasma Med. Sci.* **1** (2017) 473.

[5] https://www.caen.it/subfamilies/digitizers/.

[6] W.J. Ashmanskas et al., *Waveform-sampling electronics for a whole-body time-of-flight PET scanner, IEEE Trans. Nucl. Sci.* **61** (2014) 1174.

[7] L. Jokhovets et al., *Improved rise approximation method for pulse arrival timing, IEEE Trans. Nucl. Sci.* **66** (2019) 1942.

[8] https://www.xilinx.com/support/documentation/ip_documentation/div_gen/v5_1/pg151-div-gen.pdf.

2022 JINST 17 C04022